## **CLAIMS**

1. A method of forming a microelectronic interconnect structure containing a bilayer

Having thus described our invention in detail, what we claim is new and desire to secure by the Letters Patent is:

undefill layer comprising the steps of: 2 3 (a) forming a first polymeric material on/a surface of a semiconductor wafer having 4 5 interconnect pads disposed thereon; 6 (b) patterning said first polymeric material to provide openings that expose said 7 8 interconnect pads; 9 (c) forming conductive bump material in said openings; 10 11 (d) forming a second polymeric material over said first polymeric material and said 1.2 conductive bump material; 13 14 (e) dicing said semiconductor wafer into individual chips; and 15 Li 16

1 2.

1

17

18

19

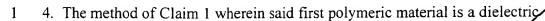
2. The method of Claim 1 wherein said first polymeric material is formed by a

material and contacts a surface of said external substrate.

(f) bonding at least on f of said individual chips to an external substrate, wherein

during said bonding said conductive bump material penetrates said second polymeric

- deposition process selected from the group consisting of spin coating, dip coating,
- 3 brushing, chemical vapor deposition (CVD) plasma-assisted CVD, sputtering, and
- 4 chemical solution deposition
  - 3. The method of Claim 2 wherein said deposition process is spin coating.



- 2 polymeric material selected from the group consisting of polyimides, polyamides, Si-
- 3 containing polymers, parylene polymers, polybenzocyclobutane and epoxies.
- 1 5. The method of Claim 4 wherein said first polymeric material is an epoxy.
- 1 6. The method of Claim 1 wherein said first polymeric material further includes an
- 2 inorganic filler.
- 7. The method of Claim 6 wherein said inorganic filler is silica, fumed silica, alumina,
- 2 titanium dioxide, glass fibers or mixtures thereof.
- 8. The method of Claim 6 wherein said inorganic filler is present in said first
- 2 polymeric material in an amount of from about 10 to about 80 wt.%.
- 9. The method of Claim 1 wherein said first polymeric material has a thickness of
- 2 from about 25 to about 100 microns.
- 1 10. The method of Claim 1 wherein said wafer is composed of a semiconducting
- 2 material and has one or more devices present therein.
- 1 11. The method of Claim 1 wherein step (b) includes lithography and etching.
- 1 12. The method of Claim 1 wherein said conductive bump material is solder.
- 1 13. The method of Claim 1 wherein said conductive bump material is applied to said
- 2 openings by injection molding, evaporation, plating, or a paste screening process.
- 1 1/4. The method of Claim 1 wherein said second polymeric material is formed by spin
- 2 /coating.





- 1 15. The method of Claim 1 wherein said second polymeric material includes a fluxing
- 2 agent and an adhesive.
- 1 16. The method of Claim 1 wherein said second polymeric material is a thermoplastic
- 2 or thermosetting adhesive.
- 1 17. The method of Claim 1 wherein said second polymeric material has a thickness
- 2 that is thinner than said first polymeric material.
- 1 18. The method of Claim 1 wherein said second polymeric material has a thickness of
- 2 from about 1 to about 10 microns.
- 1 19. The method of Claim 1 wherein said bonding step occurs a temperature of from
- 2 about 180° to about 260°C for a time period of from about 1 to about 10 minutes.
- 1 20. The method of Claim 1 wherein said external substrate is a laminate substrate, a
- 2 chip carrier, a circuit card or a circuit board, each having interconnect pads formed
- 3 thereon.

3

6

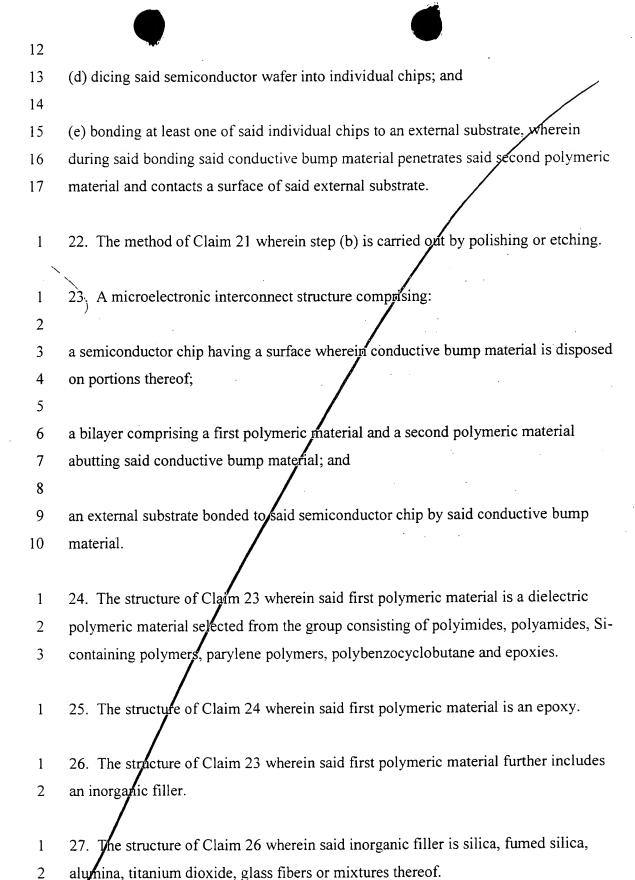
9

- 1 21. A method of forming a microelectronic interconnect structure containing a bilayer
- 2 underfill layer comprising the steps of:

4 (a) forming a first polymeric material on a surface of a semiconductor wafer having

5 conductive/bump material disposed on portions thereof;

- 7 (b) removing a portion of said first polymeric material so as to expose top surfaces of
  8 said conductive bump material;
- 10 (c) forming a second polymeric material on said first polymeric material and said exposed top surfaces of said conductive bump material;





- 28. The structure of Claim 26 wherein said inorganic filler is present in said first
- 2 polymeric material in an amount of from about 10 to about 80 wt. %.
- 1 29. The structure of Claim 23 wherein said chip is composed of a semiconducting
- 2 material and has at least one device present therein.
- 1 30. The structure of Claim 23 wherein said conductive bump material is solder.
- 1 31. The structure of Claim 23 wherein said second polymeric material includes a
- 2 fluxing agent and an adhesive agent.
- 1 32. The structure of Claim 23 wherein said second polymeric material is a
- 2 thermoplastic or thermosetting adhesive.

